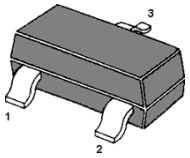
DTC143ZCA DIGITAL TRANSISTOR (NPN)

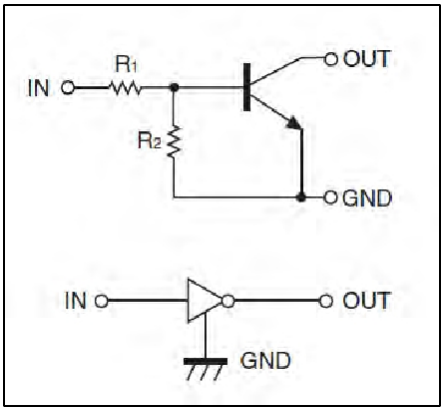
FEATURES

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors(see equivalent circuit)
- The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input.They also have the advantage of almost completely eliminating parasitic effects
- Only the on/off conditions need to be set for operation, making device design easy



1.Base (IN) 2.Emitter (GND)
3.Collector (OUT)
SOT-23 Plastic Package

MARKING:Z43



Equivalent Circuit

MAXIMUM RATINGS(Ta=25℃ unless otherwise noted)

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	50	V
V_{IN}	Input Voltage	-5～+30	V
I_O	Output Current	100	mA
P_D	Power Dissipation	200	mW
T_j	Junction Temperature	150	℃
T_{stg}	Storage Temperature	-55～+150	℃

ELECTRICAL CHARACTERISTICS (Ta=25℃ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	$V_{I(off)}$	V_{CC}=5V,I_O=100μA	0.5			V
	$V_{I(on)}$	V_O=0.3V,I_O=5mA			1.3	V
Output voltage	$V_{O(on)}$	I_O/I_I= 5mA / 0.25 mA		0.1	0.3	V
Input current	I_I	V_I=5V			1.8	mA
Output current	$I_{O(off)}$	V_{CC}=50V,V_I=0			0.5	μA
DC current gain	G_I	V_O=5V,I_O=10mA	80			
Input resistance	R_1		3.29	4.7	6.11	kΩ
Resistance ratio	R_2/R_1		8	10	12	
Transition frequency	f_T	V_O=10V,I_O=5mA,f=100MHz		250		MHz

Typical Characteristics

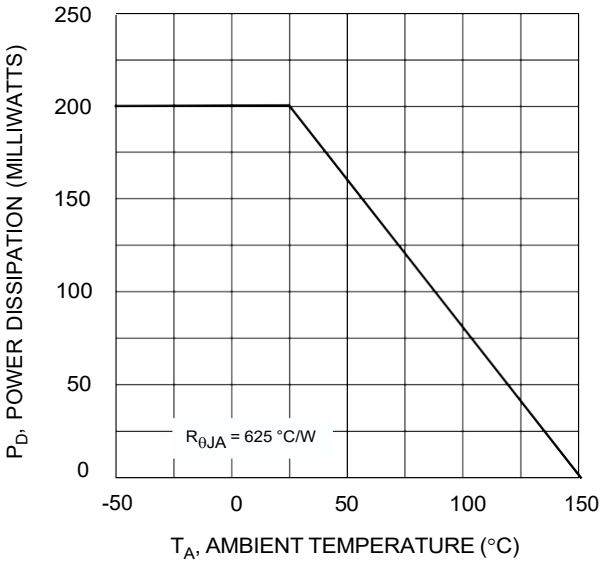


Fig. 1 Derating Curve

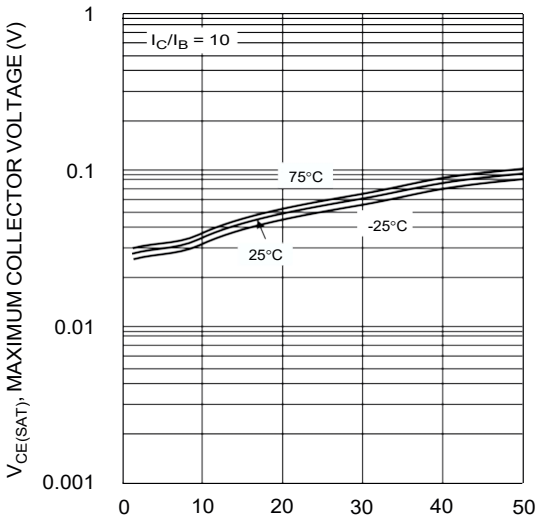


Fig. 2 $V_{CE(SAT)}$ vs. I_C

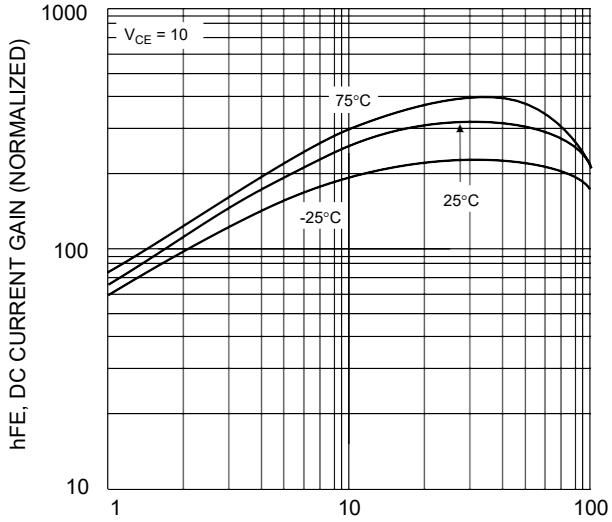


Fig. 3 DC CURRENT GAIN

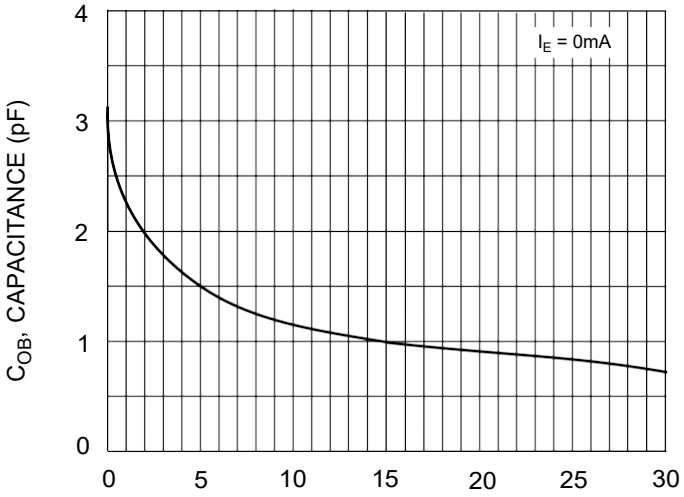


Fig. 4 Output Capacitance

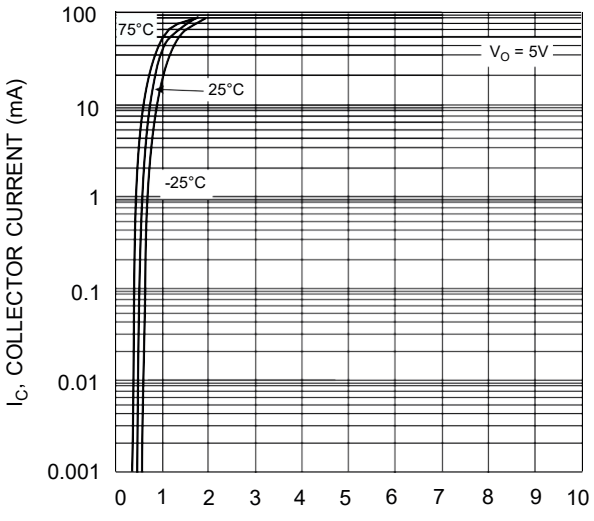


Fig. 5 Collector Current Vs. Input Voltage

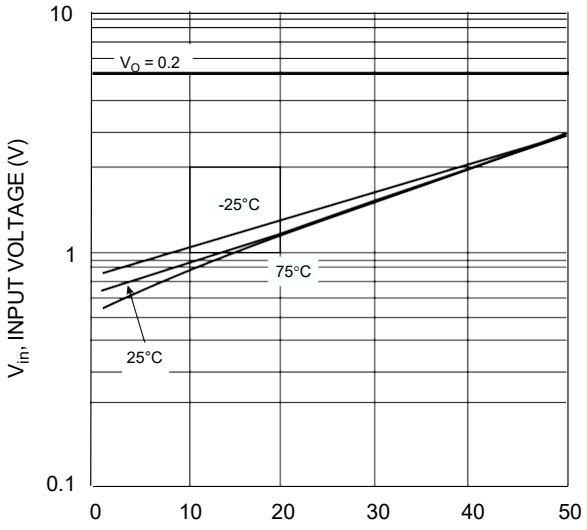
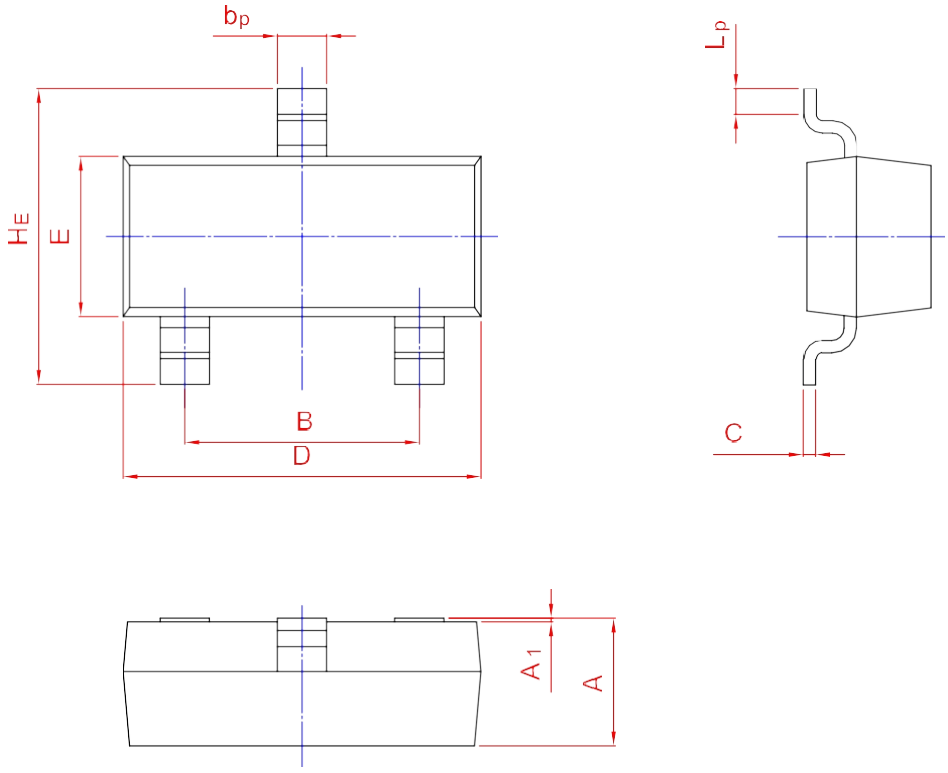


Fig. 6 Input Voltage vs. Collector Current

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT-23**



UNIT	A	B	bp	C	D	E	HE	A1	Lp
mm	1.40 0.95	2.04 1.78	0.50 0.35	0.19 0.08	3.10 2.70	1.65 1.20	3.00 2.20	0.100 0.013	0.50 0.20